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Improved Arithmetic Performance by Combining Stateful and Non-Stateful Logic in Resistive Random Access Memory 1T–1R Crossbars

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Computing-in-memory (CIM) is a promising approach for overcoming the memory-wall problem in conventional von-Neumann architectures. This is done by performing certain computation tasks directly in the storage subsystem without transferring data between storage and processing units. Stateful and non-stateful CIM concepts are recently attracting lots of interest, which are demonstrated as logical complete, energy efficient, and compatible with dense crossbar structures. However, sneak-path currents in passive resistive random access memory (RRAM) crossbars degrade the operation reliability and require the usage of active 1 Transistor–1 Resistance (1T-1R) bitcell designs. In this article, the arithmetic performance and reliability are investigated based on experimental measurements and variability-aware circuit simulations. Herein, it is aimed for the evaluation of logic operations specifically with fully integrated 1T–1R crossbar devices. Based on these operations, an N-bit full adder with optimized energy consumption and latency is demonstrated by combining stateful and non-stateful CIM logic styles with regard to the specific conditions in active 1T–1R RRAM crossbars.

1. Introduction

Processor-centric von-Neumann architectures rely on the separation of processing and storage units, with data being transferred back and forth between processing unit and the memory. This provides serious challenges for upcoming demand for data-intensive computing in terms of energy and performance. To overcome the so-called memory-wall problem, computing-in-memory (**CIM**) is one of the promising solutions. The CIM paradigm is able to perform certain logical and arithmetic operations directly within the memory bitcell array or the memory periphery. As a result, the data transfer of the operands and the results back and forth between the memory and the processing unit is reduced.[1]

Different memory technologies are used for the realization of CIM concepts. Resistive random access memory (**RRAM**) represents one of the best candidates for CIM due to their specific advantages such as complementary metal oxide semiconductor (CMOS) fabrication compatibility, good scalability, high density, and analog computations, which leads to significant performance and energy efficiency improvement.[2] The two-terminal RRAM devices (also called memristive devices) consists of a metal–insulator–metal structures with typically a metal oxide sandwiched between two metal electrodes. They are able to change their electrical resistance in a nonvolatile way dependent on the applied electric field. For most storage applications, the analog resistance range is parted into two regions, a high-resistance state (**HRS**) and a low-resistance state (**LRS**) which are assigned to the binary data values, 0 and 1.[2] Here, we focus on the subclass of filamentary oxide-based valence change mechanism (VCM) Redox resistive random access memory (VCM–ReRAM) devices,[3] as this class is becoming a mature embedded nonvolatile memory technology.[4]

RRAM-based CIM has been exploited to realize several logic and arithmetic functions.[1] However, existing CIM approaches face several major challenges, such as device integration and reliability issues. These challenges arise from single device nonidealities up to the algorithm level and, hence, pose severe restrictions both for the application and the circuit design.

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Therefore, considering and improving the reliability of designs for CIM are crucial. For the VCM–ReRAM devices, *cycle-to-cycle* (C2C) and *device-to-device* (D2D) switching variabilites as well as read instabilities[5–7] might occur which can lead to a variation in the observed device resistance or in the switching process. This possibly degrades the device performance as data storage cell or in CIM computation.[8,9] In this article, we exploit the CIM computation possibilities of co-integrated VCM–ReRAM devices with respect to their specific failure mechanisms.

2. Background

2.1. ReRAM-Based CIM

ReRAM CIM concepts exploit the unique characteristics of ReRAM devices for performing logic or arithmetic operations. As the name states, the operations are located within the data storage, i.e., ReRAM devices. For this, the ReRAM bitcells are arranged in a crossbar structure with horizontal rows and vertical columns. At each cross-junction of row and column an ReRAM bitcell is placed which stores a logic input value encoded in its resistive state.[10] A distinction is made between stateful and non-stateful CIM concepts. In contrast to more common memristive-based hardware acceleration that is used for large vector–matrix multiplications (which are also non-stateful),[11] here we focus on the realization of Boolean logic functions.

2.1.1. Non-Stateful CIM

For non-stateful concepts, either the inputs or the output are represented by a nonvolatile resistive state while the other one is a volatile state (e.g., voltage). Part of this category are sense-based non-stateful operations which are typically based on a device readout sensing and a following current comparison.[12–14] During the sensing operation, a small read voltage is applied and the device output current is measured. For this, one reference current, I_{ref}, is defined for each logic operation. If a current below this threshold is sensed, the corresponding device is classified as HRS, otherwise as LRS. This concept of device sensing can be extended to sensing multiple devices in parallel and comparing the summed current $\sum_i R_i$ to a reference current. This was proposed, i.e., in the Scouting concept.[15,16] As comparison circuitry, these concepts include analog-to-digital converters or voltage–latch sense amplifiers in the crossbar periphery. An exemplary 2-Input Scouting operation is displayed in **Figure 1**a.

The correct sensing and logic comparison depends on multiple factors, such as the RRAM R_{OFF}/R_{ON} ratio, the number of input bits, read noise, and the accuracy of the used comparator.[17] Due to the fact that the operation does not require a device switching, the influence of switching variabilities (C2C, D2D) is reduced. This marks one advantage of the Scouting CIM concepts as well as a fast operation due to the absence of a comparable slow ReRAM switching. In addition, the performed Boolean operation (i.e., AND, XOR, OR) is only set by the external classification based on the reference current, which allows a very flexible adaption and change of the operation with regard to the algorithm without any circuit modifications. The functionality of this approach has been demonstrated several times in 1T–1R nonvolatile memory structures already.[18,19] However, since the logic output is produced in the crossbar periphery, it cannot be reused for consecutive operations directly, but it requires at least temporarily storing or even an additional memory write operation to store the information permanently.

2.1.2. Stateful CIM

In stateful CIM concepts, both the output and the inputs are represented by nonvolatile resistive states. The inherent nonvolatile output storage is beneficial for using the output as input in posterior operations.[1] Prominent examples of stateful resistive concepts are the material-implication logic,[20] memristor-aided logic (MAGIC),[21] or fast and energy-efficient logic in memory (FELIX).[22] A MAGIC primitive gate is depicted in Figure 1b. It consists of (at least) two bipolar input ReRAM devices, R_1/R_2, and one output device, R_3. An input-depending resistive voltage divider forms between the inputs and the output when voltages V_{In1}/V_{In2} are applied. For certain input combinations, the output ReRAM device will selectively switch its state, if the voltage drop V_{mid} is sufficiently large. Most MAGIC-based CIM

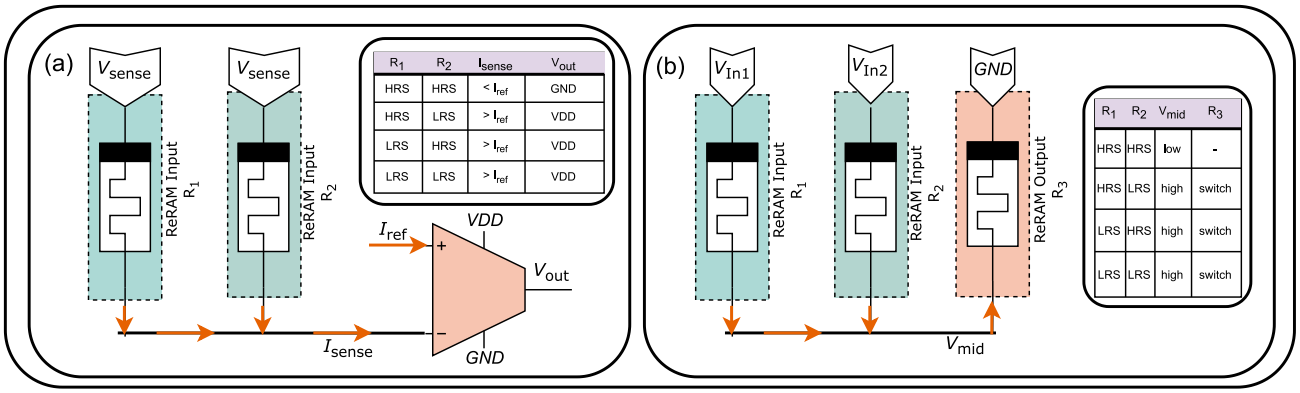

Figure 1. a) Primitive Scouting gate with two Redox resistive random access memory (ReRAM) inputs (green) and corresponding truth table for a 2-Input Scouting OR. The sensed current I_{sense} is fed into a sense amplifier (red) together with (an adjustable) reference current I_{ref}. b) Primitive MAGIC logic gate consisting of three bipolar ReRAM-based bitcells (two inputs (green) one output (red)) and corresponding truth table for a MAGIC OR.

concepts exploit the RRAM–RESET (LRS → HRS) process[23] for implementing Boolean NOR/NAND primitive gates. However, Hoffer et al. demonstrated experimentally that for RRAM technologies, which show a SET voltage $|V_{SET}|$ equal or less than the RESET voltage, $|V_{SET}| \leq |V_{RESET}|$, e.g., VCM-type ReRAM, MAGIC–RESET is not feasible and will lead to incorrect operation results.[24] In this case, the SET operation has to be exploited. With the MAGIC-SET flavor, the logic complete set of primitive Boolean gates OR (instead of NOR), NOT-material Implication (NIMP), and NOT can be implemented.

During the stateful CIM operation, the output is stored permanently within the crossbar array directly as it is produced. This reduces the necessity for additional memory operations and offers an easy reuse of the logic output for further operations. However, the RRAM switching introduces more variability in the resistive state and requires higher numbers in terms of energy and latency compared to a non-stateful readout.

2.2. Related Work and Stateful CIM Concepts

A lot of recent works have been published on the topic of implementing logic functions based on non-stateful[12–14] and stateful (see ref. [23] for a comparison) logic CIM.

Many stateful concepts[22,25–30] exploit the aforementioned MAGIC–RESET as primitive functions in passive memristive 1R-crossbars. The passive bitcell arrangement allows a flexible function mapping and cell access in both, horizontal and vertical direction. However, in passive crossbars, the issue of undesired sneak-path currents due to insufficient cell selection is critical,[31–34] which can lead to a high error rate during the operations.[35] To avoid these issues, different techniques are proposed such as half-select voltages.[36,37] The drawback of such an approach is the risk of unintended switching events and a higher energy demand.

A lesser used possibility to avoid sneak-path issues is the design of active 1T–1R memristive crossbars.[38] In these arrays, an active selector device (e.g., transistor) is added in serial connection with the RRAM device to enable an individual cell selection and protection against sneak-path currents. By adjusting the transistor gate voltage, the SET and RESET processes can also be controlled precisely. In addition, the transistor could in theory be exploited as additional logic element.[39,40]

Unfortunately, there have only been limited studies on the reliability of stateful/non-stateful CIM operations with respect to device and operation condition variabilities[41–43] in active 1T–1R crossbars. The recent works cover single CIM gate reliability issues, however lacking the challenges of larger circuit and application levels.[44]

The novelty of this work lies in the combination of experimental measurements, failure-aware modeling and statistical failure analysis of sneak-path resilient active 1T–1R crossbars for memristive CIM operations. We investigate the robustness of the single gates and the overall arithmetic by including variability and failure-aware modeling in simulations and measuring single logic gates experimentally. Furthermore, we combine stateful and non-stateful logic and exploiting the transistor-specific conditions to improve the performance for arithmetic calculations.

3. 1T–1R Single Logic Gate Evaluation

For performing logic and arithmetic CIM operations, we exploit the previously explained MAGIC–SET OR, NOT, and NIMP as stateful and the Scouting AND, OR, and XOR as non-stateful operations in 1T–1R crossbars. Due to the similar operation conditions, one peripheral circuit can be used for implementing both concepts.

3.1. Transistor-Specific Logic

As mentioned before, we aim to include the transistor in addition to being a selector device specifically as part of the logic function to achieve modified logic gates, for both stateful and non-stateful logic.

The serial connection of transistor and resistive device offers the ability to tune the whole 1T–1R path resistance not only by switching the RRAM state but also by tuning the transistor channel resistance via the applied gate voltage. This corresponds to a logic AND between the transistor gate and the RRAM state. Since both, stateful and non-stateful operations are based on the conditional resistance difference within the bitcells, this enables a novel logic paradigm for MAGIC and Scouting gate evaluation and a reduction in the required logic levels. As example, a modified logic OR gate computes to

$$X * A + Y * B \tag{1}$$

with A and B being the resistive states (HRS/0 or LRS/1) and X and Y via the applied gate voltage at the corresponding transistor (GND/0 or VDD/1) in one step. In Scouting logic, the same approach can also be extended to AND $[(X*A)*(Y*B)]$ or XOR $[(X*A) \oplus (Y*B)]$. The modified 1T–1R operation is depicted in **Figure 2**a for MAGIC–OR and Figure 2b for Scouting logic. If both transistor inputs X and Y are set to 1, this operation corresponds to the standard MAGIC/Scouting gate.

The performances of these modified gates as well as standard Scouting/MAGIC gates are tested in experimental measurements in 1T–1R crossbar structures as well as variability-aware circuit simulations. It has to be noticed that in any 1T–1R structure which features bipolar memory devices, e.g., ReRAM, the body effect in the MOSFET transistor has to be considered.[45] This effect will lead to a shift in the transistor threshold voltage and a modified current conduction through the transistor depending on the applied bulk-source voltage, V_{SB}. In the MAGIC operation the body effect marks one of several error sources which are discussed in more detail in Section 3.3.

3.2. Experimental Demonstration of 1T–1R Logic Gates

We perform several measurements on integrated 1T–1R devices based on HfO_2 ReRAM provided by the memory advanced demonstrator 200 mm (MAD200) 0.13 µm process from CEA–LETI/CMP.[46] A detailed explanation of the chip layout has already been published.[47]

A critical part for using resistive devices as logic memory is the mapping of a continuous resistance state R to a binary value 0/1. In most cases, a read-based state classification is exploited. By applying a small source voltage ($0.2\,V < V_{switching}$) and

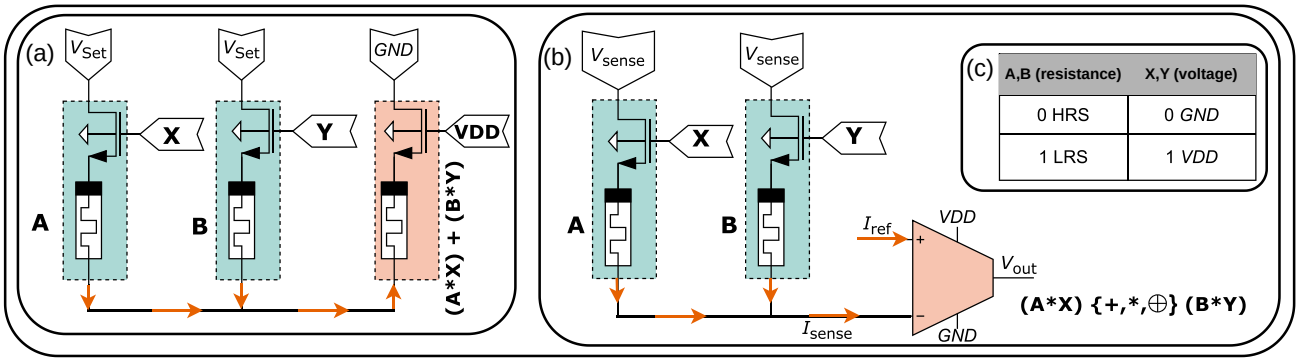

Figure 2. a) Modified MAGIC OR in 1T–1R bitcell. b) Modified Scouting AND/OR/XOR in 1T–1R bitcell. In both, MAGIC and Scouting, the transistor gates act as additional logic inputs. c) Logic encoding for resistive and voltage inputs.

measuring the resulting current I_{meas}, the RRAM resistance can be measured and thresholded, $I_{meas} \leq I_{threshold} \rightarrow 0$; else $\rightarrow 1$.

However, this measurement senses the serial resistance formed by the transistor channel resistance and the resistive device. To resolve the resistive device as best as possible, we operate the transistor in a low-Ohmic state by applying the positive suppy voltage VDD as gate voltage. **Figure 3** shows the resulting current distributions for 1T–1R measurements fitted with normal distributions. To incorporate C2C, D2D, and read variability, the data was recorded over 80 devices each cycled 100 times between HRS and LRS with three readouts in between. This yields to a total number of 24 000 datapoints per state which are displayed in Figure 3. Based on these distributions, the assignment for the resistive device states to binary values 0/1 is conducted, with $I_{meas} \leq 19.3\,\mu A \rightarrow 0$; else $\rightarrow 1$.

A similar measurement procedure is conducted for the 2-Input Scouting logic by programming two adjacent 1T–1R cells into either 0 or 1 state. Afterward, a sensing voltage is applied to both cells and the output current is measured. **Figure 4** shows the current distributions and fitted normal distributions for the standard 2-Input Scouting operations as well as selected modified gates according to Figure 2. Based on these distributions we can calculate the inherent error probabilities of the Boolean

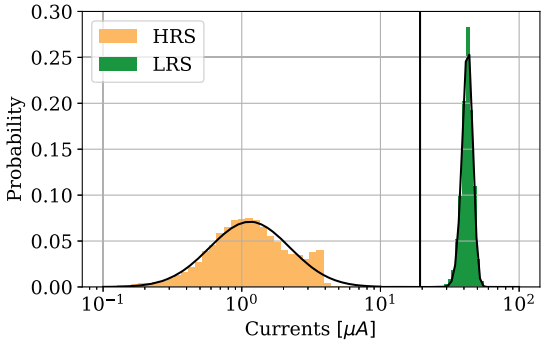

Figure 3. Measured resistance distributions of high- and low-resistive states for single 1T–1R bitcells with fitted normal distributions and marked reference current. Measurement pulses are conducted at 0.2 V. Distributions contain data from 80 different devices each cycled 100 times and read out three times with a total number of 24 000 datapoints per distribution.

operations (OR, AND) as the overlap of the fitted distributions for each expected output state. These probabilities are given in **Table 1**. Further information about the conducted statistical framework can be found in Supporting Information.

The results imply a high asymmetry between the functions. This effect arises from the fact that during a logic AND, the distinction is made between the 11-distributions and the three others. However, the spacing between this distribution and the 10/01 ones is comparable narrow, which leads to an incorrect separation between those states. In the logic OR, the 00-distribution has to be distinguished from the other three ones, which tends to be more stable due to the larger separation between 00- and 10/01/11-distributions.

A similar observation can be found for the modified Scouting operations. The high-transistor OFF-channel resistances lead to a more distinct separation between the distributions and a highly decreased failure probability, which denotes a major insight into Scouting CIM evaluation.

Due to the experimental setup, only a limited number of measurements for MAGIC logic could be performed and the corresponding failure probability can unfortunately only be estimated. Since the MAGIC operation failure depends on a conditional switching, the accurate failure probability modeling would require extensive characterization of the underlying ReRAM material stack and measurements with and without transistor which cannot be performed in the fully integrated MAD-200 chip. For MAGIC logic, we therefore performed 100 MAGIC operations according to the previously explained scheme, again for the standard Boolean combinations 00, 01, 10, 11, and selected modified combinations according to Figure 2 to demonstrate the operation principle.

To increase the switching probability in a 1T–1R MAGIC operation, two parameters can be tuned: the applied source voltage V_{Set} and the corresponding gate voltage, V_{Gate}. We measure three parameter sets, one for moderate V_{Set}/V_{Gate} and one for increase V_{Set}/V_{Gate}, respectively to investigate their influence. For these parameter sets, we perform the MAGIC–OR operation and readout the postoperation output device with previously explained LRS/HRS classification.

The measurement results in **Table 2** indicate the promising state of stateful MAGIC operations for the parameter set 3. The indented switching combinations (01, 10, 11,

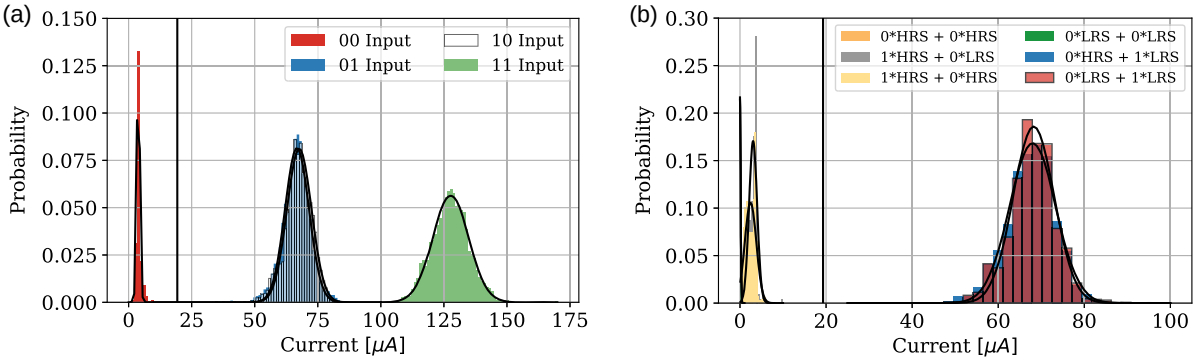

Figure 4. a) Standard 2-Input Scouting current measurements for 00, 01, 10, and 11 inputs with fitted normal distributions. The 00-distribution was scaled by a factor of 1/5 for better visibility. The data contains 512 1T–1R devices (256 programmed inputs pairs) on a MAD200 0.13 µm chip from CEA–LETI/CMP,[46] and each pair is sensed 10 times. Due to similar currents, the data sets for 01 and 10 input are overlapping significantly and merge visually (for the digital viewer, we recommend to zoom in to resolve both distributions properly). b) Modified 2-Input Scouting current measurements and corresponding fitted normal distributions for the proposed modified transistor logic. Data is sampled similar as in (a).

Table 1. Experimental failure probabilities (FPs) for Scouting OR and AND.

Standard			Modified 1T–1R	
Inputs	FP (AND)	FP (OR)	Inputs	FP (OR)
00	1.05×10^{-71}	6.23×10^{-27}	0*HRS + 0*HRS	3.73×10^{-40}
10	1.26×10^{-6}	3.79×10^{-23}	1*HRS + 0*LRS	3.40×10^{-27}
01	1.17×10^{-7}	3.09×10^{-26}	1*HRS + 0*HRS	2.14×10^{-24}
11	3.08×10^{-6}	8.9×10^{-68}	0*LRS + 0*LRS	2.37×10^{-40}
			0*HRS + 1*LRS	9.40×10^{-22}
			0*LRS + 1*LRS	2.14×10^{-26}

Table 2. Experimental switching rates (SRs) in percentage for MAGIC OR. The rates denote the number of postoperation output devices (out of 100) in LRS state. The measured parameter sets are $V_{Set}/V_{Gate} = 1.0\,V/1.5\,V$ (1), 1.2 V/1.5 V (2), and 1.0 V/1.7 V (3).

Standard				1T–1R modified	
Inputs	SR (1) [%]	SR (2) [%]	SR (3) [%]	Inputs	SR (3) [%]
00	0	0	0	0*HRS + 0*HRS	0
01	38	41	100	1*HRS + 0*LRS	0
10	55	27	99	1*HRS + 0*HRS	0
11	94	88	100	0*LRS + 0*LRS	0
				0*HRS + 1*LRS	100
				0*LRS + 1*LRS	98

0*HRS + 1*LRS and 0*LRS + 1*LRS) show a nearly 100% switching rate, while for the other input combinations, no switching occurs. Tuning the voltage parameters (V_{Set}/V_{Gate}) offers a high optimization potential toward low error rates. While the applied operation voltage V_{Set} has only a minor influence on the switching rate, the transistor gate voltage V_{Gate} marks the critical parameter for a successful switching operation. A possible explanation for this is the limited transistor current for low gate voltages, which inhibits the VCM switching process (cutoff), even for increased applied SET voltage.

Although we could not perform a full statistical failure analysis for the stateful operation due to limited experimental data, we could demonstrate of stateful CIM logic operations and their reliability beyond the prove-of-concept status.

3.3. Simulation Study of Failure Probability Dependencies

In the following, we study the failure probabilities of all proposed individual CIM logic gates with variability-aware circuit simulations based on a modified version of a previously published failure investigation framework for stateful and non-stateful CIM.[48,49] The simulation allows to investigate more complex operations which offers beneficial insights that are not accessible in the used measurements setup. To achieve this, we use the variability-aware Juelich-Aachen resistive switching tools (JART)–VCM–v1b[50] compact model for simulating VCM-type ReRAM (based on experimental HfO_2/TiO_2 from FZ Juelich[51]) devices, while for the transistors the 22 nm GlobalFoundries (GF) process design kit (PDK) was used. We conduct the active 1T–1R crossbar simulations in the Cadence Spectre environment. Furthermore to aim for realistic simulations, we include distributed parasitic elements, one resistance and capacitance per bitcell, to the crossbar design. The parasitic values as well as other simulation parameters are listed in **Table 3**. A more detailed explanation of the VCM

Table 3. Simulation parameters.

Parameters	Value
CMOS process	GF 22 nm FDX
VDD and temperature	1.5 V and 27 °C
V_{Sense} (Scouting)	0.2 V
V_{Set} (MAGIC)	1.35 V
Line resistance/capacitance	9.7 Ω/33 aF
Resistive state variation	±10%

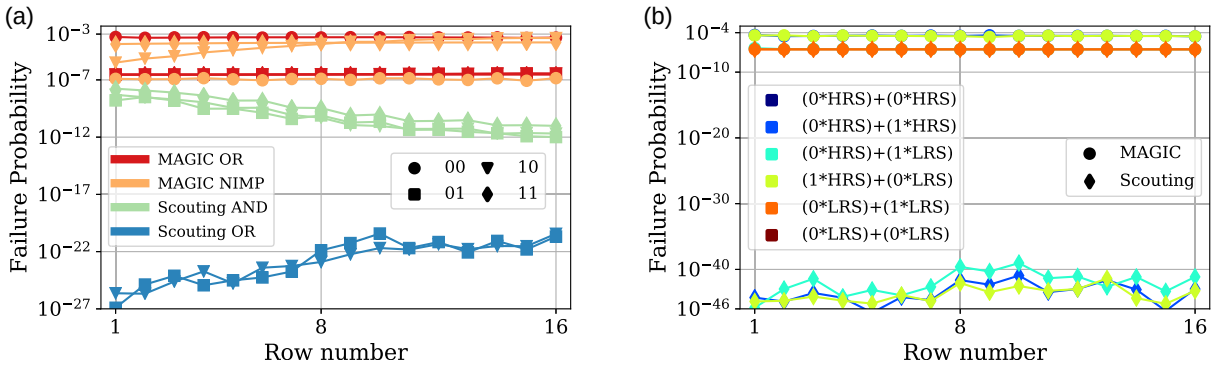

Figure 5. Simulated failure probabilities in 1T–1R crossbars for a) standard MAGIC logic gates and b) modified MAGIC logic gates with transistor as additional logic inputs. All non-depicted Scouting failure probabilities were below the simulation precision of 1×10^{-50} and not included in the figure.

model and the exploited statistical framework is given in Supporting Information.

Figure 5 depicts the resulting failure probabilities for a 16-row crossbar. For certain Scouting simulations, the calculated failure probabilities were below the simulation precision of 1×10^{-50} and are not shown in the figures. The simulation results match the experimentally observed trends, i.e., the higher failure probability for 10, 01, and 11 in standard Scouting AND. In addition, the simulated MAGIC failure probabilities match with the measured MAGIC switching rates for the optimized voltages $(V_{Set}/V_{Gate}) = (1.0\,V/1.7\,V)$. The slight deviation between simulated values and experimental results can correspond to the different technology nodes, 22 nm in simulation, and 130 nm in experiment.

The simulation results imply an input asymmetry as well as a position dependency. The position dependency has its origin in the voltage drop along one crossbar column due to circuit parasitics (e.g., line resistances), which influences the voltage-induced switching (stateful) or the sensing voltage (non-stateful). This effect could be reduced by stabilizing the voltage along one crossbar column or limiting the crossbar dimension. However, as shown in ref. [48], the failure rate asymmetry for different input combinations cannot be avoided in the MAGIC operation. The origin of this input asymmetry lies in the exploited conditional switching. To improve the switching probability for the desired input combination, the applied voltage V_{In} has to be increased. In contrast, this unavoidably leads to an increased switching probability also for the input combination where a switching is not intended. The opposing optimization between improving the switching probability and preventing a false switching is inherent for all CIM concepts which rely on a conditional device switching. Furthermore, in 1T–1R arrays the body effect in the n-type metal oxide semiconductor (NMOS) bitcell transistors has to be considered. Compared to the switching probability in passive configuration, the body effect in active 1T–1R arrangements will lead to a reduced overall switching of the output device due to the voltage degradation in the SET direction. These effects have to be taken into account for the optimization of the crossbar for both reliability and performance. For instance, the effect of asymmetric input failure can be improved by modifying the order of consecutively performed operations. To reduce the influence of the NMOS body effect, the operation voltage and/or the gate voltage can be increased or larger transistors (higher $\frac{W}{L}$) could be used. By this, we find an operation parameter set which will minimize the overall operation failure probability.

4. Combined Stateful and Non-Stateful Arithmetic Concept

Based on the aforementioned set of primitive logic gates (stateful and non-stateful), we designed an efficient carry-ripple adder (CRA).

4.1. CRA

Other CIM adders such as parallel prefix adders (Ladner-Fischer,[12] Sklanksy,[52] Koggle-Stone) have been proven to have a logarithmic dependency of the computation delay on the number of bits N, which makes them faster in general. However, proposed architectures require either highly specialist periphery[52,53] or read–write back loops and a huge number of devices, which makes them impractical.[12] Our proposed CRA offers an area-efficient design with a minimum of required devices while still being faster than comparable stateful concepts. This is achieved by splitting the calculation in a stateful and non-stateful part. The stateful evaluation is used for computing necessary intermediate values which are used in multiple operations. Also the addition SUM (S) is evaluated statefully since the sum is the important addition results. The CARRY-Out (C_{out}) is calculated in a non-stateful manner since each CARRY-Out bit is only required in one following step. This mixed concept combines the inherent advantages of stateful (nonvolatile evaluation, permanent storage) and non-stateful (fast, less variability).

The N-bit CRA is based on the representations for SUM and CARRY-Out (C_{out}) bit shown as follows:

$$\begin{aligned} C_{out} &= \overline{C_{in}} * (A*B) + C_{in} * (A+B) \quad (I) \\ S &= C_{in} * (\overline{A \oplus B}) + \overline{C_{in}} * (A \oplus B) \quad (II) \end{aligned} \tag{2}$$

with C_{in} the CARRY-In bit and $*$, $+$, $\oplus$ the Boolean functions AND, OR, and XOR, respectively. For the MAGIC–SET primitive

Table 4. Logic gate representations for the SET-based standard MAGIC operation.

Logic gate	Symbol	Representation in MAGIC–SET
OR(A,B)	$A + B$	OR(A,B)
NOT(A)	$\overline{A}$	NOT(A)
NIMP(A,B)	$A \nrightarrow B$	NIMP(A,B)
AND(A,B)	$A * B$	NOT(NOT(A) OR NOT(B))
XOR(A,B)	$A \oplus B$	NIMP(A,B) + NIMP(B,A)
XNOR(A,B)	$\overline{A \oplus B}$	NOT (NIMP(A,B) + NIMP(B,A))

Table 5. Failure of the simulated full adder accuracy for different bit lengths N.

Number of bits	Absolute failure	Relative failure
N	Per addition	Per addition
2	2.97×10^{-5}	4.94×10^{-6}
4	1.19×10^{-4}	3.96×10^{-6}
8	2.01×10^{-3}	3.94×10^{-6}
16	6.16×10^{-1}	4.70×10^{-6}

The absolute failure and relative failure per addition. Relative failure is calculated as absolute failure divided by maximum output for the addition of two N-bit numbers $2^{N+1} - 2$.

operations, **Table 4** lists the corresponding Boolean gate representations. The logic truth tables for the used gates and further information are presented in Supporting Information.

For an N-bit full adder calculation, the operations according to the representations in Equation (2) split into three parts: 1) **storing** two N-bit input numbers A,B in binary representation, 2) obtaining the input-dependent factors $(A*B)/(A+B)/(A\oplus B)/(\overline{A\oplus B})$ **(Pre-Steps)**, and 3) concatenating them with the CARRY-Inputs, $C_{\text{in}}/\overline{C_{\text{in}}}$ **(Calculation)**.

During the Pre-Steps, MAGIC–SET operations based on the primitive standard MAGIC set {OR, NIMP, NOT} are performed which store the results directly as the resistive state of the output RRAM cell. Since the Pre-Step operations for each bit are independent of the bit position, they can be performed for all N bits in parallel, exploiting the column-wise operation structure in 1T–1R crossbars.

Afterward, the Calculation phase is initialized by setting the CARRY input as $C_{\text{in},1} = 0 \rightarrow \overline{C_{\text{in}}} = 1$ for the first bit. Starting at this point, the first SUM bit S_1 is calculated according to Equation (1) statefully and stored in another crossbar column. For this step, the proposed modified MAGIC operation is exploited where the CARRY inputs $C_{\text{in},1}, \overline{C_{\text{in}}}$ are applied as gate voltages. The advantage of this 1T–1R logic is directly visible by comparing the structures of Equation (1) and (2) II, as both hold two ANDs, concatenated by an OR.

From this point, the CARRY bit $C_{\text{out},1}$ is calculated via a modified non-stateful Scouting in a similar manner with Equation (2) I and set as new CARRY input $C_{\text{in},2} = C_{\text{out},1}$. This flow of SUM (stateful writing) and CARRY (volatile sensing) calculation is repeated for all N bits consecutively, which results in the CRA typical step-like, cascading procedure. The vector representation of this concept is shown in **Figure 6**.

4.2. Accuracy Validation

The proposed N-bit CRA flow based on the cascading logic scheme is validated based on a probabilistic simulation. For one addition run, two N-bit inputs are drawn from a random distribution and stored as inputs. At each point in Pre-Steps and Calculation, the single-gate failure probabilities from Figure 5 are used to simulate the gate output in accordance to the input values and the crossbar position. The achieved $N + 1$ bit output value is then compared to the theoretical expected value and the failure is measured for the full adder.

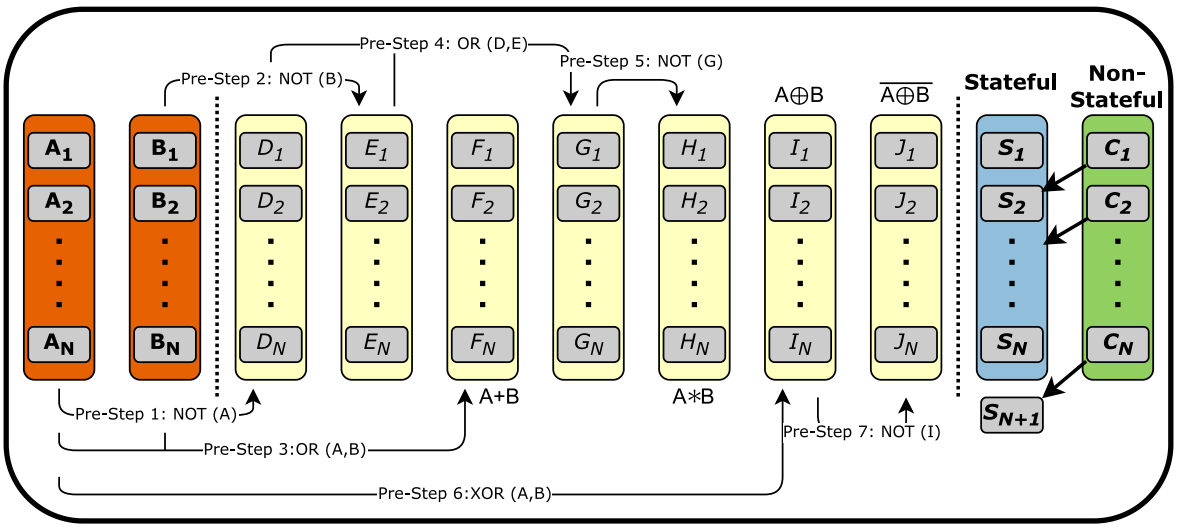

Figure 6. Abstracted flow for logic operations on vectors in proposed carry-ripple adder. A and B represent the N-bit input vectors and D–J represent the Pre-Step operation results. These are used together with the non-stateful CARRY vector C to calculate S, the resulting N + 1-bit SUM vector.

Table 6. Comparison of proposed concept with benchmarks of state-of-the-art N-bit full adders.

Logic primitives	Crossbar	Circuit area	Steps	Result state	References
	Type	No. RRAM	Cycles		
NOT/MAJORITY	1T–1R	$6 \times (8N + 16)$	$4 \times \log_2(N) + 6$	Voltage	[12]
Scouting				Volatile	
NOT, AND, OR	1S–1R	$12N - 1$	$12N + 1$	Resistance	[52]
CRS-Logic				Nonvolatile	
NOR, NAND	1T–1R	$14N$	$13N$	Resistance	[56]
MAGIC				Nonvolatile	
XOR/MAJORITY	1T–1R	$5N$	$2N + 2$	Voltage	[57]
Scouting				Volatile	
NOR/NOT	1R	10×3	$20N + 15$	Resistance	[58]
MAGIC				Nonvolatile	
RIMP, NIMP, XOR	1R	$2(N + 1)$	$2(N + 1) + 2$	Resistance	[54]
CRS-Logic				Nonvolatile	
NOT, NIMP, OR	1T–1R	$10N + 1$	$8 + N(Write) + N(Read)$	Resistance	This work
MAGIC/Scouting				Nonvolatile	

For a bit of length $N = [2, 4, 8, 16]$, we simulated $M = 1 \times 10^7$ additions and calculated additions and calculated the absolute failure per addition as $\frac{\sum_i (x_i - y_i)^2}{M}$, with x_i/y_i the theoretical/simulated addition results. Since the absolute failure has only limited meaning, e.g., a deviation of ± 1 on a 2-bit addition is worse than ± 1 for a 16-bit addition, we also calculate the relative failure per addition by dividing the absolute failure by possible addition range $2^{N+1} - 2$. The results in **Table 5** show an increasing absolute failure for higher N while the relative failure remains constant.

4.3. Comparison to Other Memristive Adders

In this subsection, we compare our proposed full adder design to various other state-of-the-art N-bit CIM-based full adder concepts, in terms of required cells and cycles. This is shown in **Table 6**.

The comparison shows that the proposed vector-based 1T–1R architecture and the combination of non-stateful and stateful operations offer a unique trade-off between required circuit area and latency. Although pure non-stateful concepts such as provided in ref. [12] are inherent faster due to different adder architectures and multi-bit operations, the volatile output and the required CMOS periphery for logic computation and storing marks a significant disadvantage. While the complementary resistive switching (CRS)-logic approach[54] shows a better performance, during the CRS computation the inputs are overwritten, which terminates a reuse of the original addition inputs.

5. Conclusion

We demonstrate two exemplary resistive CIM logic families, namely Scouting and MAGIC, experimentally and in failure-aware simulations to estimate their operation reliability. We extend each operation by exploiting the transistor gate in resistive 1T–1R structures as additional logic input and based on single logic gates we propose a combined stateful/non-stateful CIM CRA. Achieving the operation result as nonvolatile resistance states while replacing intermediate steps with faster and error-tolerant non-stateful operation can be an important step toward reliable and CMOS competitive CIM. Possible applications for such an arithmetic structure are standalone systems with a limited chip area and only occasional but unavoidable computations. Due to the nonvolatile memory, resistive device can reliably store data without power-consuming refreshing and conduct operations only if necessary. Furthermore, the measured low experimental failure probabilities emphasize the promising aspects of non-stateful and stateful resistive CIM concepts based on industrial-grade 1T–1R devices. The obtained accuracy results are highly promising with respect to state-of-the-art static RAM (SRAM) CIM designs[55] which spend significant resources for error correction and reliability. Compared to the advanced SRAM technology, the upcoming nonvolatile ReRAM memories offer a huge potential of reliable and energy efficient CIM.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

1T–1R logics, computing-in-memory, resistive devices, valence change mechanism, Redox resistive random access memory (VCM–ReRAM)

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